Remarks

In the Office Action, the Examiner noted that Claims 1-36 are pending in the application, and that Claims 1-36 are rejected. By this amendment, Claim 1 has been amended. Thus, Claims 1-36 are pending in the application. The Examiner's rejections are traversed below.

Rejection Under 35 USC 112, First Paragraph

Claim 1, stands rejected under 35 USC 112, first paragraph. The Examiner alleges that the specification does not adequately describe "predefined subset." Applicants respectfully contend that the specification teaches with sufficient scope "predefined subset" such that one of ordinary skill, in programming using HDL languages to model IC devices, to make and/or use the invention without undue experimentation. One of ordinary skill in the art knows that an HDL language representation of a particular device includes code representing structure, logical interconnections, physical layout, characteristics (e.g., capacitance, resistance, propagation delay), and/or the like, depending upon the level of abstraction (e.g., functional, RTL, gate, transistor, layout, or mask level). Predefined subsets are generic (e.g., non-case specific) behavioral descriptions which do not include non-ATPG related information such as timing and physical layout information (page 14, lines 14-17; page 16, lines 5-9; and page 17, lines 19-21). Furthermore, the reduction from a behavioral description to a simplified behavioral description is shown between 400 of Figures 4, and 600 of Figure 6A. One skilled in the art would understand how to make and/or use predefined subsets for use in converting behavioral descriptions into simplified behavioral descriptions

without any additional details. Thus, Applicants respectfully request withdrawal of this rejection.

Claim 2, stands rejected under 35 USC 112, first paragraph. The Examiner contends that the specification does not adequately describe "excludes timing information." Applicants respectfully contend that the specification teaches with sufficient scope "excludes timing information" such that one of ordinary skill, in programming using HDL languages to model IC devices, to make and/or use the invention without undue experimentation. One of ordinary skill in the art knows that an HDL language representation of a particular device includes code representing structure, logical interconnections, physical layout, characteristics (e.g., capacitance, resistance, propagation delay), and/or the like, depending upon the level of abstraction (i.e. functional, RTL, gate, transistor, layout, or mask level). One skilled in the art would understand how to make and/or use predefined subsets by excluding timing information for use in converting behavioral descriptions into simplified behavioral descriptions without any additional details. Thus, Applicants respectfully request withdrawal of this rejection.

Claim 3, stands rejected under 35 USC 112, first paragraph. The Examiner contends that the specification does not adequately describe "excluding physical layout information." Applicants respectfully contend that the specification teaches with sufficient scope "excludes physical layout information" such that one of ordinary skill, in programming using HDL languages to model IC devices, to make and/or use the invention without

undue experimentation. One of ordinary skill in the art knows that an HDL language representation of a particular device includes code representing structure, logical interconnections, physical layout, characteristics (e.g., capacitance, resistance, propagation delay), and/or the like, depending upon the level of abstraction (i.e. functional, RTL, gate, transistor, layout, or mask level). One skilled in the art would understand how to make and/or use predefined subsets by excluding physical layout information for use in converting behavioral descriptions into simplified behavioral descriptions without any additional details. Thus, Applicants respectfully request withdrawal of this rejection.

Claim 12, stands rejected under 35 USC 112, first paragraph. The Examiner contends that the specification does not adequately describe "displaying a graphical representation of said primitives." Applicants respectfully contend that one skilled in the art would understand how to graphically display the simplified behavioral descriptions based upon the primitives descriptions and their logical interconnection contained in the simplified behavioral descriptions. Furthermore, the drawings are replete with examples (e.g., Figures 6A, 7A-7C, 10, 11A-11F). Thus, Applicants respectfully request withdrawal of this rejection.

Claims 13 and 25, stand rejected under 35 USC 112, first paragraph. The Examiner contends that Claims 13 and 25, are "computer readable medium" and "computer controlled electronic design automation systems" claims, respectively, with the same limitations as Claim 1, and therefore are

rejected for the same reasons. To the extent that Claims 13 and 25, may correspond to the method Claim 1, Applicants respectfully contend that they are enabled for the same reasons as Claim 1. Thus, Applicants respectfully request withdrawal of these rejections.

Claims 14 and 26 stand rejected under 35 USC 112, first paragraph. The Examiner contends that Claims 14 and 26, are "computer readable medium" and "computer controlled electronic design automation systems" claims, respectively, with the same limitations as Claim 2, and therefore are rejected for the same reasons. To the extent that Claims 14 and 26, may correspond to the method Claim 2, Applicants respectfully contend that they are enabled for the same reasons as Claim 2. Thus, Applicants respectfully request withdrawal of these rejections.

Claims 15 and 27, stand rejected under 35 USC 112, first paragraph. The Examiner contends that Claims 15 and 27, are "computer readable medium" and "computer controlled electronic design automation systems" claims, respectively, with the same limitations as Claim 3, and therefore are rejected for the same reasons. To the extent that Claims 15 and 27, may correspond to the method Claim 3, Applicants respectfully contend that they are enabled for the same reasons as Claim 3. Thus, Applicants respectfully request withdrawal of these rejections.

Claims 24 and 36, stand rejected under 35 USC 112, first paragraph. The Examiner contends that Claims 24 and 36, are "computer readable

medium" and "computer controlled electronic design automation systems" claims, respectively, with the same limitations as Claim 12, and therefore are rejected for the same reasons. To the extent that Claims 24 and 36, may correspond to the method Claim 12, Applicants respectfully contend that they are enabled for the same reasons as Claim 12. Thus, Applicants respectfully request withdrawal of these rejections.

Rejection Under 35 USC 112, Second Paragraph

Claim 3, stands rejected under 35 USC 112, second paragraph. The Examiner alleges that it is unclear how a simplified behavioral model can exist without implicit physical layout information. The Applicants respectfully submit that the Examiner is confusing physical layout with logical interconnections. Physical layout information concerns the X-Y-Z orientation of the device upon the semiconductor substrate (e.g., the length width and depth of an implanted n-region forming a drain of a device). Physical layout characteristics are not utilized for automatic test generation. Thus, Applicants respectfully request withdrawal of this rejection.

Claims 15 and 27, stand rejected under 35 USC 112, second paragraph. The Examiner contends that Claims 15 and 27, are "computer readable medium" and "computer controlled electronic design automation systems" claims, respectively, with the same limitations as Claim 3, and therefore are rejected for the same reasons. To the extent that Claims 15 and 27, may correspond to the method Claim 3, Applicants respectfully contend that they

are definite for the same reasons as Claim 3. Thus, Applicants respectfully request withdrawal of these rejections.

No Prior Art Examination – Indefinite Claims

Claim 3, 15 and 27, stand rejected under 35 USC 112, first paragraph for lack of enablement and under 35 USC 112, second paragraph for indefinite claims. The Examiner alleges that it would be counter-productive to make speculative assumptions about the meanings of Claims 3, 15 and 27, for the purpose of examination against prior art. The Applicants respectfully contend that Claims 3, 15 and 27, are enabled and definite for the above-stated reasons. Therefore, Applicants respectfully request examination of Claims 3, 15 and 27, against prior art without further delay.

The Examiner also states that Claims 3, 15 and 27, stand rejected under 35 USC 101, for lack of utility. Applicants respectfully assert that the Examiner has not articulated a prima facie case of lack of utility under 35 USC 101, in the present office action. Applicants furthermore contend that the present invention has utility by providing an improved method for converting hardware descriptive language primitives used in designing circuits, into primitive suitable for use in automatic test pattern generation systems used in testing the fabricated devices.

Rejections Under 35 USC 102 and 103

Claim 1, stands rejected under 35 USC 102(b), as being anticipated by Beausang US Patent 5,696,771. Applicants respectfully assert that the Examiner has failed to make a prima facie showing of anticipation. Anticipation requires that 1) a single reference, 2) that teaches or enables, 3) each of the claimed elements and functional limitations, 3) expressly or inherently, 5) as interpreted by one of ordinary skill in the art. Furthermore, for each element and functional limitation, the relied upon reference must also teach each feature and/or structure of the element and/or limitation.

The Examiner alleges that Claim 1, is an independent claim with three limitations. For ease of analysis, Applicants have amended Claim 1, to clearly identify each element, limitation, specific feature and/or structure of the claim. The Applicants respectfully contend that amended Claim 1, is an independent claim with eleven (11) elements: a structural model; a memory; an automatic test pattern generator (ATPG); a simulation model; a simulation library; a computer system memory; a behavioral hardware description language; a simplified behavioral model; a predefined subset; a computer system; and a plurality of ATPG memory primitives. Claim 1, also includes nine (9) functional limitations: accessing; wherein said simulation model is described in a behavioral hardware description language; generating; by re-describing said memory with a predefined subset; translating; automatically; under control; wherein said structural model comprises a plurality of ATPG memory primitives; and storing. To the extent

that the above listed elements and/or limitations may not comprises elements or functional limitations, they comprise specific features and or structure of the claims.

Furthermore, Applicants respectfully submit that Beausang teaches a method of electronic design automation utilizing hardware descriptive language. In particular the method provides for the logical designing of circuits that provide for testing of the physical circuits. The method includes replacing memory cells in the netlist with memory cells that specially designed to apply and observe test vectors to and from portions of the integrated circuit. These designed memory cells specially designed for test are called scannable memory cells. (col. 2, line 66, through col. 3, line4).

Alghough both Beausang and the present invention begin with some form of HDL descriptions, Beausang utilizes the descriptions to design circuits. In so doing, non-scannable memory primitives are replaced with scannable memory primitives. The insertion of scannable memory primitives, however, typically results in a circuit that no longer meets the required area, power, timing and the like constraints. Therefore, Beausang teaches a method of un-scanning memory primitives until an acceptable logical circuit design is achieved.

An automatic test generation procedure is then utilized to generate test vectors to test the physical circuit. The problem that the present invention solves is that the hardware descriptive language primitives cannot

be used by the, conventional art, automatic test generation procedures. Thus, the present invention teaches a method for converting hardware descriptive language primitives to a form suitable for use in automatic test generation procedures, which create test vectors for testing various physical circuits.

Applicants also assert that the "constraint driven scan insertion" of Beausang is not equivalent to "generating a simplified behavioral model" as taught by the present invention. The "constrain driven scan insertion" (Fig 8, element 655) is fully described in: Figure 10, Figure 11, column 20 line 29 through column 25 line 12. From the description it is clear that constrain driven scan insertion is an iterative process of un-scanning violated memory cells and scanning non-violated memory cells to optimize testability of the circuit while meeting various constraints.

"Generating a simplified behavioral model" as taught in the present application comprises removing various parts of the hardware descriptive language primitive to form an automatic test generation primitive. Removing the parts of the hardware descriptive language primitive, such as timing and physical layout characteristics, is not equivalent to un-scanning violated memory cells and scanning non-violated memory cells.

Thus, Examiner has failed to make a prima facie case that Beausang anticipates Claim 1, of the present invention, by showing that Beausang discloses each and every element, functional limitation, feature, and/or structure. Withdrawal of this rejection is respectfully requested.

Claims 4-12, stand rejected under 35 USC 102(b), as being anticipated by Beausang US Patent 5,696,771. Applicants respectfully submit that Claims 4-12, depend from patentable independent Claim 1, and incorporate all the limitation thereof. Thus, Claims 4-12, are also patentable over Beausang. Withdrawal of this rejection is respectfully requested.

Claims 13 and 16-24, stand rejected under 35 USC 102(b), as being anticipated by Beausang US Patent 5,696,771. The Examiner contends that Claims 13 and 16-24, are "computer readable medium" claims with the same limitations as Claims 1 and 4-12, respectively, and therefore are rejected for the same reasons. To the extent that Claims 13 and 16-24, may correspond to the method Claims 1 and 4-12, Applicants respectfully contend that they are not anticipated for the same reasons as Claims 1 and 4-12. Thus, Applicants respectfully request withdrawal of these rejections.

Claims 25 and 28-36, stand rejected under 35 USC 102(b), as being anticipated by Beausang US Patent 5,696,771. The Examiner contends that Claims 25 and 28-36, are "computer controlled electronic design automation" claims with the same limitations as Claims 1 and 4-12, respectively, and therefore are rejected for the same reasons. To the extent that Claims 25 and 28-36, may correspond to the method Claims 1 and 4-12, Applicants respectfully contend that they are not anticipated for the same reasons as Claims 1 and 4-12. Thus, Applicants respectfully request withdrawal of these rejections.

Claims 2, 14 and 26, stand rejected under 35 USC 103(a), as being obvious in view of Beausang US Patent 5,696,771, and Wohl and Waicukauski, "Using Verilog Simulation Libraries for ATPG. Applicants respectfully submit that Claims 2, 14 and 26, depend from patentable independent Claims 1, 13 and 25, respectively, and incorporate all the limitation thereof. Thus, Claims 2, 14 and 26, are also patentable over Beausang, and Wohl and Waicukauski. Withdrawal of this rejection is respectfully requested.

Conclusion

For all the reasons advanced above, Applicant respectfully submits that the application is in condition for allowance and that action is earnestly solicited. The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

The Commissioner is hereby authorized to charge any additional fees, which may be required for this amendment, or credit any overpayment, to Deposit Account 23-0085.

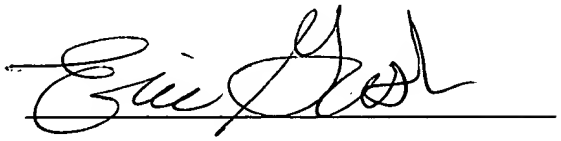
In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to

charge any fee for such an extension of time or credit my overpayment for an extension of time to Deposit Account 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: September 9, 2002



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VERSION WITH MARKING TO SHOW CHANGES MADE

In the Specification

At page 8, lines 19-21:

Figure 4 is a simplified formal description of a memory port using an exemplary subset of Verilog in accordance with one embodiment of the present invention.

At page 15, line 25, through page 16, line 3:

Automatic generation of structural descriptions from table-based descriptions is described in ~~co-pending~~ U.S. Patent ~~application serial~~ No. ~~09/052,998~~ 6,148,436, ~~filed~~ issued on ~~March 14, 1998~~ November 14, 2000, entitled "Automatic Generation of Gate-Level Descriptions from Table-Based Descriptions for Electronic Design Automation," by Peter Wohl, assigned to the assignee of the present invention, and is incorporated herein by reference.

In the claims

1. A method of constructing a structural model ~~for~~ of a memory for use in an ATPG (Automatic Test Pattern Generation), said method comprising the steps of:

accessing a simulation model of said memory, from a simulation library stored in ~~memory of~~ a computer system memory, wherein said simulation model is described in a behavioral hardware description language;

generating a simplified behavioral model of said memory by re-describing said memory with a predefined subset of said behavioral hardware description language; ~~and~~

~~under computer control, automatically~~ translating, automatically and under control of a computer system, said simplified behavioral model into said structural model of said memory, ~~and storing said structural model in said memory~~ wherein said structural model comprises a plurality of ATPG memory primitives; and

storing said structural model in said computer system memory.

In the drawings

See attached redlined sheets.